## REMARKS

Claims 1-28, all the claims pending in the application, stand rejected upon informalities and on prior art grounds. Claims 1-28 stand rejected upon informalities under 35 U.S.C. §112, first paragraph. Claims 3-4, 10-11, and 18-19 stand rejected upon informalities under 35 U.S.C. §112, second paragraph. Applicants respectfully traverse these rejections based on the following discussion.

### I. The 35 U.S.C. §112 Rejections

#### A. The rejection of claims 1-28 under 35 U.S.C. §112, first paragraph.

The Applicants respectfully disagree with the position that support is not found in the specification for the language "wherein said target spacer width controls an amount of diffusion of said dopant into a channel region of said substrate below said gate conductor", which was previously amended into independent claims 1, 9, 16, and 24.

Specifically, paragraph [0004] of the specification explains that typically gate height can not be reduced because "implanting dopants with a sufficient energy to dope the source and drain regions and for halo formation using the polygate as a self-aligned mask can cause the dopants to penetrate through the poly gate and the gate dielectric into the channel as the gate height is decreased". Thus, with regard to the claimed invention, paragraph [0039] indicates the gate height can be reduced because "the sacrificial layers 14-16 allows a sufficiently high-energy-implantation ... to be utilized for doping not only the gate but also the source, drain, and halo regions without [vertical] impurity penetration through the gate oxide 12 into the channel region of the silicon 11."

Paragraph [0005] further explains that gate height can also not typically be reduced because "with a shorter gate height, the maximum size of the spacer is reduced due to the reduced step height for the RIE (reactive ion etch) of a deposited spacer material of a given thickness, resulting in lateral encroachment of S/D dopants and a higher probability of silicide bridging between the gate and the S/D." More specifically, paragraph [0006] explains that "impurities can diffuse into the channel" from "extension and source and drain implants" during "RSD processing".

Thus, paragraph [0036] refers to the "target spacer width" as a design element of the invention. More specifically, paragraph [0030] indicates that the "sacrificial layer at the top of the gate stack allows the formation of larger disposable spacers", that the "invention uses a two-step spacer formation process for spacer width modulation..." and that "[w]ith the larger spacers, the invention also avoids the dopant encroachment... problems that can occur when the reduced gate height limits and decreases the achievable size of the spacers...". For example, paragraph [0031] provides that the "width of the spacer is made relatively larger" ... in order to give more room for boron diffusion" and that "larger disposable spacers" are used to "minimize any effects of lateral encroachment of boron". Similarly, paragraph [0050] provides that without the sacrificial layers, the "gate height would make it difficult to form a disposable spacer large enough to separate the raised source and drain regions from the gate sidewall" and that "with the larger spacers, the invention also avoids the dopant encroachment and silicide bridging problems that can occur when reduced gate heights decrease the size of the spacers."

Therefore, while the specification does not explicitly state that the target spacer width controls an amount of diffusion of the impurity (i.e., dopant) this feature would be implicitly understood by one skilled in the relevant art given the above-cited information contained in the specification. However, to further clarify this feature of the invention, as disclosed in the specification, independent claims 1, 9, 16 and 24 are amended to reflect that the spacers with the target spacer width separate the source and drain regions from the gate stack so as to avoid lateral encroachment of the impurity into a channel region below the gate stack. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections of claims 1-28.

**B. The rejection of claims 3-4, 10-11, and 18-19 under 35 U.S.C. §112, second paragraph.**

The patentable features of dependent claims 3, 10 and 18 have been moved to independent claims 1, 9, and 16, respectfully. Thus, claims 3, 10 and 18 are canceled herein. Claims 4, 11, and 19 are amended to address instances of indefiniteness.

## II. The Prior Art Rejections

Claims 1-28 again stand rejected under 35 U.S.C. §102(b) as being anticipated by Park, et al. (U.S. Patent No. 6,429,084), hereinafter referred to as Park. Applicants respectfully traverse these rejections based on the following discussion.

Regarding independent claim 1, Park does not teach or suggest the following features: (1) that "by forming said gate stack from said laminated structure with said at

least one sacrificial layer, as opposed to without said at least one sacrificial layer, a height of said gate stack is increased so that said target spacer width can be achieved" and (2) "doping regions of said substrate not protected by said spacers with an impurity to form source and drain regions adjacent said gate stack, wherein said spacers with said target spacer width separate said source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack."

Similarly, regarding independent claims 9, 16 and 24, Park does not teach or suggest the following features: (1) that "by forming said gate stack from said laminated structure with said at least one sacrificial layer, as opposed to without said at least one sacrificial layer, a height of said gate stack is increased so that said target spacer width can be achieved" and (2) "wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process and wherein said spacers with said target spacer width separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack."

Additionally, with regard to independent claims 16 and 24 Park does not teach or suggest that "said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities".

As discussed in the July 18, 2005 amendment, the cited prior art and the present invention each provide methods for forming CMOS transistors with raised source and drain regions; however, the problems addressed are different as are the processes used to solve the problems. Park addresses the problem of unwanted overgrown epi growth on

the gate and STI but not reduced gate height and, thus, does not address the ability to form large enough spacers to avoid unwanted lateral diffusion of dopants. (Note that while the remarks section of the previously filed amendment included a statement to the effect that Park addressed the problems associated with reduced gate height, upon further review of Park it has been determined that the statement was incorrect and is, therefore, withdrawn.)

More particularly, Park discloses a method of forming CMOS transistors with raised source and drain regions (col. 1, lines 5-6). In the Park method a gate stack is formed with several sacrificial layers above the gate conductor (col. 1, lines 58-62). The sacrificial layers protect the surface of the gate conductor during subsequent processing. A protective nitride layer is deposited over the substrate and the gate-sacrificial layers (col. 1, lines 66-67). Temporary spacers are formed on the protective layer against the gate stack and a width of the spacers is "set to define the area for the halo and extensions implants" (col. 2, lines 1-5). A portion of the protective layer 60 above the substrate is etched to define the source and drain regions and then, the temporary spacers are removed (col. 2, lines 25-30). Then, the source and drain regions 34 are implanted, although this step can be omitted if the source and drain regions were previously implanted (col. 2, lines 33-34; see Figure 5). Column 2, lines 34-37 provide that "the layer 60 is thick enough to block the implant in the region that will contain the extension implant." After the source and drain regions 34 are implanted in the substrate, raised source and drain regions are epitaxially grown (col. 2, lines 43-47; see Figure 7). Unwanted epi growth is prevented by the remaining nitride layer on the gate stack and

adjacent to the gate stack in the area of the substrate designated for the S/D extension. Then, after additional processing steps, extension and halo implantation is performed (col. 2, lines 48-64), which also implants the raised epitaxially grown source and drain regions.

Park *does not* address the issue of lateral encroachment of the impurities (i.e., dopants) from the source and drain regions 34 through the substrate into the channel region below the gate conductor. Specifically, Park only mentions at col. 2, lines 1-5 that the widths of the spacers that are formed adjacent to the gate conductor are "set to define the area for the halo and extensions implants." Park also indicates that the nitride layer is thick enough to block penetration by the dopant through the nitride layer down into the area of the substrate designated for the halo and extensions implants (col. 2, lines 34-37). However, Park discusses neither the height of the gate conductor alone nor the overall height of the gate stack, and thus, does not consider that the sacrificial layers have a purpose other than protection of the gate conductor. Specifically, Park does not consider or disclose that the sacrificial layers are added to the gate stack so as increase the height of the gate stack (i.e., to achieve a specific height) that allows a target spacer width to be achieved and, thereby, avoid lateral diffusion of the S/D dopants into the channel region.

In response to the Applicants' previous arguments, the Office Action refers to the fact that the Park drawings do not actually illustrate impurities under the gate conductor as support for the position that the temporary spacers in Park protect the channel region. However, as mentioned above, since reduced gate height was not addressed by Park, the problem of lateral encroachment would not need to have been considered by Park.

Additionally, support for the fact that lateral diffusion of dopants was not even considered by Park is found in the fact that not only do the drawings fail to show lateral diffusion of impurities into the channel region but also fail to show any lateral diffusion of impurities at all. Those skilled in the art would recognize that such lateral diffusion would necessarily occur to some extent, especially following the epi growth process. Thus, the lack of lateral dopant diffusion into the extension region and under the gate stack in the Park drawings only supports the fact that lateral diffusion was not considered by Park and not the idea that the spacers were designed with a target spacer width so as to avoid lateral encroachment of the source and drain impurities into the channel region.

Therefore, the Applicants respectfully submit that Park does not teach or suggest the similar features of independent claims 1, 9, 16 and 24 of forming spacers with a target spacer width, wherein the spacers with the target spacer width separate the source and drain regions from the gate stack so as to avoid lateral encroachment of the impurity into a channel region below the gate stack.

Furthermore, regarding independent claims 9, 16 and 24, Park does not teach or suggest "wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process and wherein said spacers with said target spacer width separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack" (see paragraphs [0042] and [0047]). Specifically, Park discloses implanting the source and drain regions in the substrate *before growing the epi* (col. 2 lines 33-48, see Figure 5).

The impurities implanted into these source and drain regions in the substrate would necessarily be subjected to the epi process (col. 2, lines 44-48, see Figure 7) with a conventional temperature range from about 750°C-850°C) and, thus, subjected to the deleterious effects of transient enhanced diffusion of impurities, such as boron. Col. 2, lines 56-58 and associated Figures 9-10 of Park disclose that after the epi is grown a second implant process is used to implant dopants into the halos, extensions and a section of the epi, but not into the source and drain regions in the substrate below the epi (which were previously implanted).

Regarding independent claim 16 and 24, Park further does not teach or suggest "wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities". Contrarily, as mentioned above, Park teaches doping the source and drain regions in the substrate prior to growing the epi on those source and drain regions (see Figures 5-7 and associated text in the Specification). Thus, Park necessarily teaches that the process of epitaxially growing the raised source and drain regions is performed in the presence of doping impurities.

Therefore, the Applicants respectfully submit that independent claims 1, 9, 16, and 24 are patentable over the prior art of record. Further, dependent claims 2-8, 10-15, 17-23 and 26-28 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of

the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

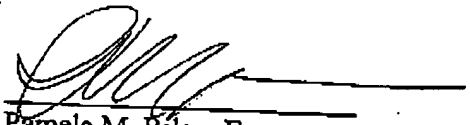
## III. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-24, and 26-28, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,



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Pamela M. Riley, Esq.
Registration No. 40,146

Gibb I.P. Law Firm, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (410) 573-0227
Fax: (301) 261-8825
Customer Number: 29154